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Design of Area Efficient Binary Counter Based Multistage LFSR

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Abstract:

Especially compared to conventional binary counters, The Linear Feedback Shift Register Counter is a well-known technology in Wide Assortment counters because which can diminish the circuit's complexity as well as ensure continuous improvement. As a necessary consequence, deciphering the Linear Feedback Shift Register pattern is indeed a challenging issue, you'll need a lot of logic for pseudo - random pattern order into binary format, which necessitates the use of specialized logic circuits. This broadsheet offers a Multi stage LSFR counter design which uses proposed LFSR counter with sequence logic as well as binary counters. Combination of these two counters will give the better presentation in terms of performance and area without compromising latency as well as power as existing counter. Four bit pattern generated Multi stage LFSR counter is implemented in this architecture by utilizing Xilinx 14.7 version.

Keywords: Linear Feedback Shift Register, decoding logic, binary counter, as well as event counters.

I.INTRODUCTION

Shift registers are a form of sequential logic circuit used in digital electronic circuitry, mainly for storage of digital data set up in a linear fashion which has its inputs connected to outputs in such a way that the data is shifted down the line when the circuit is activated. The shift register with continuous feedback has an incoming bit which would be the outcome of a continuous model of 2 or many of its existing phases.

A shift register having a regular combination of its previous condition in computations is characterized as a linear-feedback shift register. The much more popular scalable feature using specific components is exclusive-or (XOR) gating component. Linear Feedback Shift Registers which were extensively utilized in both hardware and software.

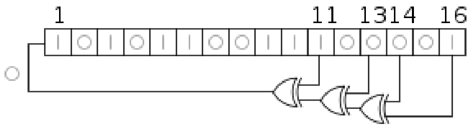


Fig.1 Linear Feedback Shift Register

Linear Feedback Shift Registers are widely adopted among both hardware as well as software.

On the other hand, a Linear Feedback Shift Register (LFSR) with such an appropriately constructed feedback mechanism and seeding could start generating a stream of characters that seems to be randomized and also has a tremendous amount.

The linear feedback shift registers, which are discussed in the classic method, generate pseudorandom number generators, it has been shown that they are an appropriate method of delivering synchronous counters as well as are very well adapted for large array implementations, as the shift registers can function as a mechanism for serial reading.

The count order of linear feedback Shift Registers, however, is pseudorandom, so additional processing is needed to decode onto binary order of the LFSR sequence.

LFSR sequence is decrypted into binary pattern we have three dissimilar methodologies are implemented: 1. Iteration method, 2. Direct look up table method as well as 3. Time-memory trade-off algorithm. The method of iteration iterates over the linear feedback shift registers count sequence as well as relates to the counter value.

In system on chip (Soc) layouts, deciphering individual cell in the array in binary order is required for the further computation. This requirement implies that the deciphering logic should be both comprehensive as well as fast due to the numerous mechanisms which must happen. Furthermore, every one of the aforementioned approaches improve appropriately with the size of the LFSR in both time as well as field. A most of the array based technologies like this would have been impossible to make utilizing Linear Feedback Shift Register counters (LFSR) however if they were utilized for single-photon detection, need excessively high integrated Look up Tables.

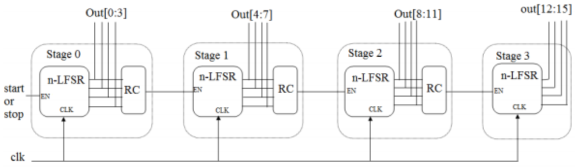


Fig. 2. Block diagram of the multistage LFSR counter.

The modern counter design results from multiple LFSR stages is proposed in this study, which can be deciphered utilizing logic that expands logarithmically instead of exponentially with the counter size. A simple concatenation with linear feedback shift registers counters which are similar to the binary ripple counters which will decrease the outcome substantially. This investigation presents a way for spreading the ripple signal in time, as well as a modified logic deciphering framework which allows this.

This broadsheet offers a Multi stage LSFR counter design which uses proposed LFSR counter with sequence logic as well as binary counters. Combination of these two counters will give the better presentation in terms of performance and area without compromising latency as well as power as existing counter.

II. EXISTING METHOD

The counter's architecture is depicted in schematic form. An active signal has been used to control M equivalent blocks of n-LFSR. Whenever the (m-1)th n-LFSR encounters a state change, the active signal is affirmed, as well as the mth n-Linear Feedback Shift Register advances to that phase. The space of M*n bit state which allows to traverse. The counter could also be utilized as a high-speed serial readout loop of large array architectures.

The Linear Feedback Shift Register counter is divided into Min dependent modules, allowing every n-LFSR to be decoded independently by a n*n bit LUT rather than a (M*n) bit Look Up Table. For small n, we can implement LUT on a chip.

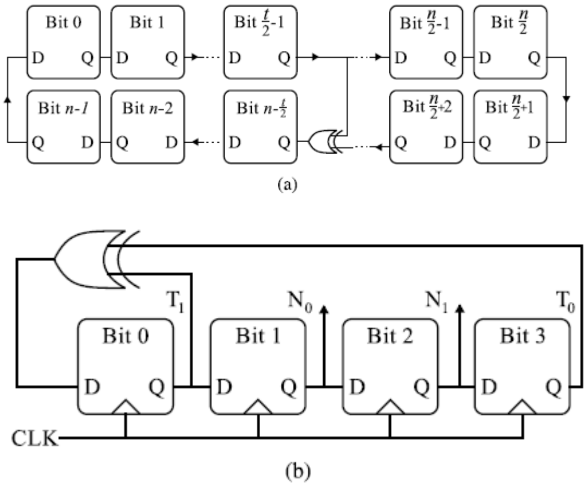


Fig. 3. (a) Structure of a conventional *n*-bit ring generator. (b) Structure of conventional many-to-one 4-LFSRs.

Because every counter phase is engaged within one cycle of the previous step, missing phases from either the Linear Feedback Shift Register series would cause enormous blocks of counter phases to be disregarded. It is therefore essential to get the n-LFSR equipped for maximum duration. An n-maximum LFSR's sequence length is only 2n − 1, thus extra logic is necessary for integrate the missed state into count sequence. It can be done by disabling the feedback logic when the 0x000 with both the NOR and XOR operations. .1 status has been observed. This pattern-extension logic stretches the pattern length to 2n of the individual parts LFSRs so that any state throughout the state space of 2Mn is protected by the counter.

It also makes it possible to use the multi-stage counter in applications requiring coverage of every state, such as self-starting counters, where conventional LFSRs would not be applicable. Through fairly minimal logic which overrides the LFSR feedback as well as ripple-carry blocks, which is accomplished. A multi-level counter diminishes the counter to Min-dependent elements, permitting every n-Linear Feedback Shift Register to also be deciphered independently utilizing an n-bit LUT rather than a (M*n)*(M*n) bit Look Up Table. For modest n, the LUT could be simply integrated upon on chip.

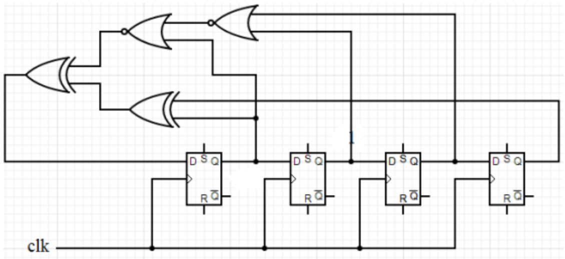


Fig.4 The configuration of a multi-stage n-LFSR block with sequence-extension logic

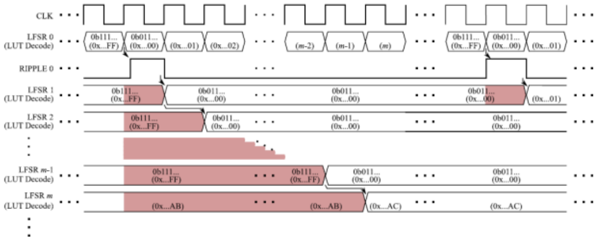


Fig. 5. Timing diagram for ripple-carry logic

Ripple-Carry Logic:

In the Linear Feedback Shift register the transformation of 0b1111 _0b0111, every phase of dynamical system included in this. In the n-LFSR implementation, this is an appropriate conversion from propagate triggering. The commencement of the sequence for n-LFSR is modified as 0b0111....., resulting in a deciphering logic of 0 x....00.

The ripple signal would have to propagate over every phase and identify whether another stage would emigrate. Furthermore, for every successive phase added to the counter, the propagate signal is transferred to the next clock cycle for subsequent stages. Which applies the m clock cycle delay to the transition edge for the mth step while delivering the transition edge across time.

The ripple-carry logic's functioning is revealed by the counter timing description. So each Linear Feedback Shift Register state is characterized as a binary representation (0b...), however the deciphered state of the Look Up Table (LUT Decipher signal) appears to be the bracket hex value (0x... When LFSR 0 turns 0b1111. To the condition 0b0111. A ripple 0 signal is generated in this state. At the following clock edge, the RIPPLE 0 signal operates on LFSR 1, allowing it to pass via 0b1111. Transformation 0b0111. As a consequence, a ripple signal is transmitted for the upcoming clock edge to act on Linear Feedback Shift Register 2. In this way, the ripple-carry logic disruptions the transition edge by one clock cycle every level.

The delayed transformation leads to the creation of an error triangle, as seen by the outlined states.

Those individuals appear to be inaccurately decoded by Look Up Table as well as a small amount of deciphering functionality has been done.

Decoding Logic:

The array performance of multistage LFSR counter as well as the decoding logic serves as a postponed stage. Why because the LFSR value must be considered from the list, it is communicated via a LUT. The LUT converts most states into binary order. As a result, sufficient logic is necessary to repair the problems caused by delayed transition.

Overspill errors arise if there is an error in the earlier stage so it is equal to 0x….FF. Such faults suggest that on an earlier clock cycle, a previous stage could have triggered a ripple occurrence.

A decoding logic which recognizes those errors as well as corrects them. Every stage error detection relies on the deciphered value of a preceding stages, so that every stage is performed consecutively. Unless the subsequent stage's fault condition is recognized, the wrong register of next stage is set to rectify the next clock cycle. The defects are either the Look Up Table outcome is retrieved by the upcoming erroneous step nor which one is adhered to a LUT response, either which one is applied to the Look Up Table outcome.

If indeed the primary point is faulty, the upcoming point will have an excess flaw as well as also 0x...FF. It can be identified through ANDing the carryout of the increase with the invalid register of next point. Subsequent foibles could be acknowledged through keeping earlier deciphered stages in latches as well as contrasted these with a counter which keeps track of the current phase value.

A counter tends to count to M, thus it needs bits of y = [log2 (M)]. Consequently, just a correlation of y-bits among the previously deciphered should be developed.

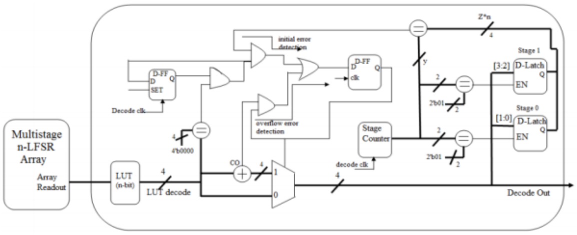


Fig. 6. Logic to decode the multistage LFSR counter state order into binary. Each stage is decoded separately in sequence.

A time for counting value to be deciphered will rely both on M as well as n. The decoding logic introduces one clock cycle per counter stage, thus to decode the whole count value, M clock cycles are provided. The decoding logic for critical path is integration, but theoretically involves the LUT, an incrementer, as well as the stage counter relation, which have all decreased outcome for large n.

Hence, for greater n values, the maximum clock rate will be diminished.

Unless the array is read sequentially, therefore the decryption logic can be established in the read chain as a pipeline. It just contributes to a whole array readout for M clock cycle pipeline delay, however all individual counter values would be read out with a deciphered value.

II. PROPOSED METHOD

It has been suggested which Linear Feedback Shift Register as well as binary counters be employed in a multiple stage counter system. Whenever these dual counters were integrated, the outcome is a stronger infrastructure with the same functionality than the prior architecture.

The four-stage system is modified in this proposal, with the first bit is made up of a Linear Feedback Shift Register, while the following bits are made up of a binary counter. As a result of this setup, the performance was superior than the current architecture. One Linear Feedback Shift Register as well as three binary counters are suggested as components in this survey for a four-phase multi-stage counter. The Linear Feedback Shift Register counter is utilized in the first step, as well as the binary counters are used in later stages. To avoid performance deterioration, ripple carry logic is added among two counters.

The outcome values of the acknowledged counter, as well as the fulfillment of a sequence of bits, are utilized in ripple-carry logic. Figure 7 illustrates the suggested counter.

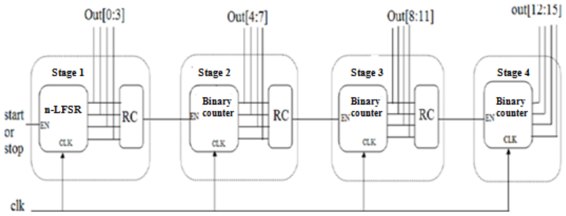


Figure 7: proposed multistage LFSR counter design

The output of an n-bit LFSR is pseudo random in the first stage. In single photon applications, the LFSR pseudo random count must be converted to binary order. The results of the first step can be used in testing applications, while the remaining phases are employed in counter applications. This job was completed through decoding logic. This suggested counter uses the same decoding logic as the existing multistage counter.

Binary counter:

A counter is a device in electronic circuits as well as computation that maintains the couple of times a specific outcome as well as procedure has performed, frequently in conjunction to a timer. The much more popular method is a sequential digital circuit's circuitry, which has numerous outcome lines as well as a clock input line.

One of the most common uses for the flip - flops is as a counter. The counter's outcome comprises a predetermined state depending on the clock pulse. This counters outcome could be used to calculate the number of pulses.

Counters are divided into the following categories:

- Counters that are asynchronous,
- Counters that are synchronized.

Counters have been utilized to monitor events in a variety of digital electronic applications. A counter is a circuit that operates in a sequential manner. The term counter refers to a digital circuit that counts pulses. The most common use of flip-flops is on the counter. A clock signal is applied to a collection of flip-flops.

The synchronous as well as asynchronous counters were classed as follows, depending on how the counting proceeds: Counters should be raised. Counters are lowered. Counters that go up as well as down. Flip-flops, also known as latches, are primary ingredients in digital circuitry that function as a type of storage device, storing the state of single bit. Digital state machines can be built by combining numerous flip-flops.

This binary counter is essentially a state machine device which rotates via its configurations throughout response to every clock cycle. The J - k flip is the most ubiquitous switch architecture why because it could be utilized to explore a wide variety of switch done by altering how the values of J as well as K ports are interconnected.

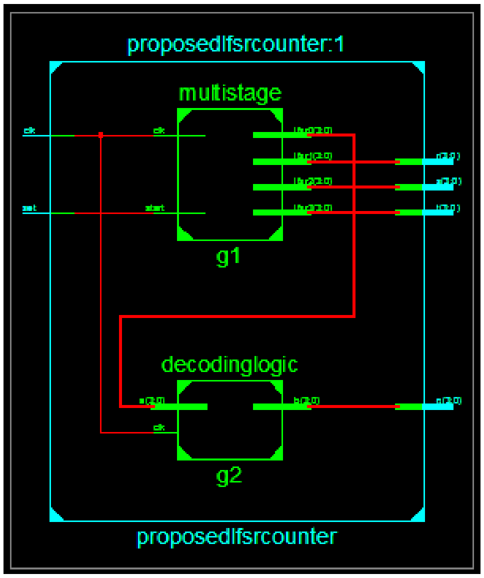
A counter is a device in electronic circuits as well as computation that maintains the couple of times a specific outcome as well as procedure has performed, frequently in conjunction to a timer.

The flip-flops are utilized with a toggling function in this illustration, which implies the outcome alterations for every complex clock cycle. Ones are fed into both the J as well as K pins of the flip-flops to accomplish this. The outcome will never alter if all the J as well as K terminals are set to zero, irrespective of the supply. As a consequence, all of the J & K pins could be used as an enable signal for this kind of circuit.

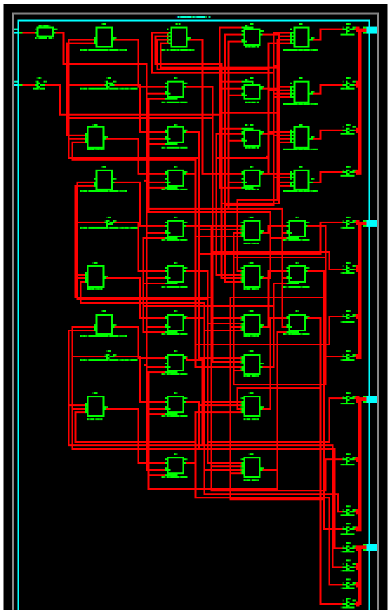
III. RESULTS AND DISCUSSSION

The proposed design has better area when compared to existing design without degrading the other factors. In the proposed method while we are using binary counter in three it will decrease the area, improve the performance of the architecture.

The proposed multi stage Linear feedback shift register with multi stage counter as well as existing multi stage counter both are functionally verified by using Xilinx ISE 14.7 version tool.

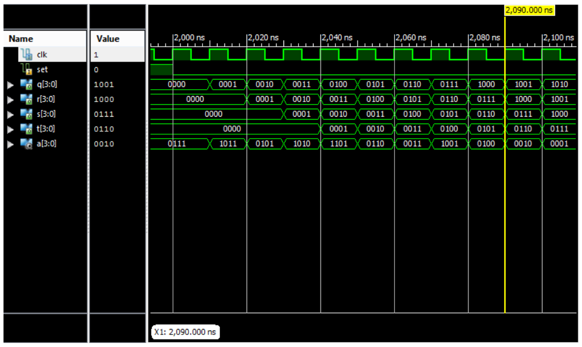


RTL Schematics



Technology Schematics

Simulation Results:



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Name      Value   |2,000 ns      |2,020 ns      |2,040 ns      |2,060 ns      |2,080 ns      |2,100 ns
clk       1
set       0
q[3:0]    1001    0000   0001   0010   0011   0100   0101   0110   0111   1000   1001   1010
r[3:0]    1000    0000          0001   0010   0011   0100   0101   0110   0111   1000   1001
s[3:0]    0111    0000                 0001   0010   0011   0100   0101   0110   0111   1000
t[3:0]    0110    0000                        0001   0010   0011   0100   0101   0110   0111
a[3:0]    0010    0111   1011   0101   1010   1101   0110   0011   1001   0100   0010   0001
```

Evaluation of Area, Delay and Power report:

	Area	Delay(ns)	Power(w)
Existing	23	5.406	0.034
Proposed	20	5.406	0.034

CONCLUSION

This work describes a simplified design as well as implementation of a multiple stage counter, as well as the deciphering logic expected to drive the count sequence in to the binary format. In this research we are implementing the multi-stage linear feedback shift register counter which employs both LFSR as well as binary counters. The functional verification done by utilizing Xilinx ISE 14.7 version tool among the existing multi stage LFSR as well as suggested linear feedback shift counter. According to the above conclusions, the suggested architecture consumes less space than that of the previous architecture while sustaining the same delay as well as power.

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